TSMC-99-374/408B

OIPE JC174 JAN 04 2002 PATENT & TRADEMARK OFFICE

December 10, 2001

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To: Commissioner of Patents and Trademarks
Washington, D.C. 20231

Fr: George O. Saile, Reg. No. 19,572
20 McIntosh Drive
Poughkeepsie, N.Y. 12603

Subject: Serial No. 09/978,227 10/16/01

Chih-Chung Chiu

LOW RESISTANCE SELF ALIGNED EXTENDED GATE STRUCTURE UTILIZING A T OR Y SHAPED GATE STRUCTURE FOR HIGH PERFORMANCE DEEP SUBMICRON FET

Grp. Art Unit: 2812

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56. Copies of each document is included herewith.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231, on December 13, 2001.

Stephen B. Ackerman, Reg.# 37761

Signature/Date 12/13/01

U.S. Patent 5,053,849 to Izawa et al., "Transistor with Overlapping Gate/Drain and Two-Layered Gate Structures", discloses an overlapping gate/drain tow layer gate structure.

The following technical reports discuss high performance gate structures:

1) Lin et al., "A Novel Self-Aligned T-Shaped Gate Process for Deep Submicron Si MOSFET's Fabrication", IEEE Electron Device Letters, Vol.19, No. 1, January 1998, pp. 26-28.
2) A. Chatterjee et al., "Sub-100nm Gate Length Metal Gate NMOS Transistors Fabricated by a Replacement Gate Process", IEEE, c. 1997, journal not identified.
3) Wakabayashi et al., "A High-Performance 0.1um CMOS with Elevated Salicide using Novel Si-SEG Process", IEEE, c. 1997, journal not identified.
4) Hisamoto et al., "A Low-Resistance Self-Aligned T-Shaped Gate for High-Performance Sub-0.1-um CMOS", IEEE transactions on Electron Devices, Vol. 44, No.6, June 1997, pp. 951-956.

U.S. Patent 5,817,558 to Wu, "Method of Forming a T-Gate Lightly-Doped Drain Semiconductor Device", describes a T-shaped gate formed of amorphous silicon.

U.S. Patent 5,559,049 to Cho, "Method of Manufacturing a Semiconductor Device", discloses a T-gate structure with a single poly layer and capacitively coupled auxiliary side gates.

The following two U.S. Patents describe a T-gate made of contact metal:

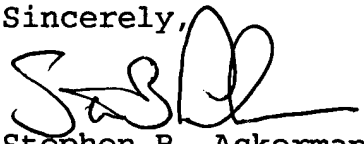
1) U.S. Patent 5,856,232 to Yang et al., "Method for Fabricating T-Shaped Electrode and Metal Layer Having Low Resistance".
2) U.S. Patent 5,288,660 to Hua et al., "Method for Forming Self-Aligned T-Shaped Transistor Electrode".

U.S. Patent 5,585,307 to Yoo, "Forming a Semi-Recessed Metal for Better EM and Planarization Using a Silo Mask", discloses a Y-shaped gate.

U.S. Patent 5,688,704 to Liu, "Integrated Circuit Fabrication", discloses a T-gate and silicide process.

U.S. Patent 4,939,071 to Barrera et al., "Method for Forming Low Resistance, Sub-Micrometer Semiconductor Gate Structures", discloses a T-gate process.

Sincerely,



Stephen B. Ackerman,
Reg. No. 37761

Form PTO-1449

INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(Use several sheets if necessary)

OIPE JC17 JAN 0 4 2002 PATENT & TRADEMARK OFFICE

Docket Number (Optional)	Application Number
TSMC-99-304/408B	09/978,227
Applicant: Chih-Chung Chiu	
Filing Date: 10/16/01	Group Art Unit: 2812

U. S. PATENT DOCUMENTS

Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date if Appropriate
	5053849	10/1/91	Izawa et al.	357	59	4/25/90
	5817558	10/6/98	Wu	438	291	12/10/97
	5559049	9/24/96	Cho	437	44	7/25/95
	5856232	1/5/99	Yang et al.	438	574	7/5/96
	5288660	2/22/94	Hua et al.	437	187	2/1/93
	5585307	12/17/96	Yoo	437	187	2/27/95
	5688704	11/18/97	Liu	437	41	11/30/95
	4939071	7/3/90	Barrera et al.	430	314	3/6/84

FOREIGN PATENT DOCUMENTS

	Document Number	Date	Country	Class	Subclass	Translation YES	Translation NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

Lin et al., "A Novel Self-Aligned T-Shaped Gate Process for Deep Submicron Si MOSFET's Fabrication", IEEE Electron Device Letters, Vol. 19, No. 1, Jan. 1998, pp. 26-28.

A. Chatterjee et al., "Sub-100 nm Gate Length Metal Gate NMOS Transistors Fabricated by a Replacement Gate Process, IEEE, c.1997, journal not identified.

Examiner	Date Considered

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant

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Applicant: Chih-Chung Chin	
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